Amendments to the Claims:

Please amend claims as follows. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (previously presented) A method of receiving encoded and then shuffled data in a communication system supporting multi-level demodulation, comprising the steps of:

demodulating received data according to a predetermined demodulation scheme and outputting a modulation symbol having a predetermined number of code symbols;

deshuffling the code symbols in a deshuffling order corresponding to shuffling, the deshuffling order being determined considering the demodulation scheme and a structure of a deshuffling memory device; and

reading the deshuffled code symbols, decoding the code symbols at a predetermined code rate, and outputting a packet.

2. (previously presented) The method of claim 1, wherein in the deshuffling step, the code symbols are stored at write addresses in the deshuffling memory device, which are generated according to a selected one of a plurality of predetermined demodulation schemes using a corresponding one of a plurality of formulas wherein

i) if QPSK, then $WA=(SA+2xmi+ci) \bmod P_{MAX}$,

ii) if 8-PSK, then if $ci=0$, $WA=(SA+mi+2N_{SP}/3) \bmod P_{MAX}$

else $WA=(SA+2xmi+ci-1) \bmod P_{MAX}$,

iii) if 16-QAM, then if $ci \bmod 2=0$, $WA=(SA+2xmi+ci/2+N_{SP}/2) \bmod P_{MAX}$

else $WA=(SA+2xmi+ci/2) \bmod P_{MAX}$, and

wherein WA is a write address, SA is a start address depending on the index of received packet data, mi is the index of a demodulated symbol, ci is the index of a code symbol in the demodulated symbol, N_{SP} is the length of the received packet data, P_{MAX} is the maximum bit

index of packet data generated from a code sequence according to a packet size, and mod represents a modulo operation.

3. (original) The method of claim 1, wherein in the code symbol deshuffling step, the code symbols are separated into systematic symbols with a relatively high priority and parity symbols with a relatively low priority, and the systematic symbols and the parity symbols are stored in separate memories.

4. (original) The method of claim 3, wherein the code symbol deshuffling step further comprises the steps of:

generating temporary addresses according to the deshuffling order considering the demodulation scheme;

generating write addresses using the temporary addresses considering the separate memories; and

storing the code symbols at the write addresses in the separate memories.

5. (original) The method of claim 1, wherein the code symbol deshuffling step comprises the steps of:

separating the code symbols into systematic symbols with a relatively high priority and parity symbols with a relatively low priority, and storing the systematic symbols and the parity symbols in separate memories;

generating temporary addresses according to the deshuffling order according to the demodulation scheme ;

generating write addresses using the temporary addresses considering the separate memories; and

storing the code symbols at the write addresses in the separate memories.

6. (previously presented) The method of claim 5, wherein the temporary addresses are generated according to a selected one of a plurality of predetermined demodulation schemes using a corresponding one of a plurality of formulas wherein

i) if QPSK, then $TA=(SA+2xmi+ci) \bmod P_{MAX}$,
ii) if 8-PSK, then if $ci=0$, $TA=(SA+mi+2N_{SP}/3) \bmod P_{MAX}$
else $TA=(SA+2xmi+ci-1) \bmod P_{MAX}$, and
iii) if 16-QAM, then if $ci \bmod 2=0$, $TA=(SA+2xmi+ci/2+N_{SP}/2) \bmod P_{MAX}$
else $TA=(SA+2xmi+ci/2) \bmod P_{MAX}$;

wherein TA is a temporary address, SA is a start address depending on the index of received packet data, mi is the index of a demodulated symbol, ci is the index of a code symbol in the demodulated symbol, N_{SP} is the length of the received packet data, P_{MAX} is the maximum bit index of packet data generated from a code sequence according to an packet size, and mod represents a modulo operation.

7. (currently amended) The method of claim 5, wherein if the packet is 408, 792 or 1560 bits, the write addresses are generated according to at least one formula selected from

i) if $0<TA<N_{EP}$, *then*
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0),

ii) if $N_{EP}<TA<3xN_{EP}$, *then*
Input Symbols=P0 or P0', WA=TA-N_{EP}*, and Write to MEM1 (MEM_CS=1)*, and

iii) if $3xN_{EP}<TA<5xN_{EP}$, *then*
Input Symbols=P1 or P1', WA=TA-3xN_{EP}*, and Write to MEM2 (MEM_CS=2)*;

wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]]<u>P0/P0'</u> denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a

final write address, MEM_CS is a memory select signal, and MEM0, MEM1 and MEM2 denote first, second and third memories, respectively.

8. (currently amended) The method of claim 5, wherein if the packet is 2328 bits, the write addresses are generated according to at least one formula selected from

i) if 0<TA<N_{EP}*, then*
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0),

ii) if N_{EP}*<TA<3x*N_{EP}*, then*
if ((TA-N_{EP}*) mod 2=0), then*
Input Symbols=P0, WA=(TA-N_{EP}*)/2, and Write to MEM1 (MEM_CS=1)*
else
Input Symbols=P0', WA=(TA-N_{EP}*)/2, and Write to MEM2 (MEM_CS=2)*, and

iii) if TA>3xN_{EP}*, then*
if ((TA-3xN_{EP}*) mod 2=1), then*
Input Symbols=P1', WA=(TA-3xN_{EP}*)/2+2328, and Write to MEM1 (MEM_CS=1)*
else
Input Symbols=P1, WA=(TA-3xN_{EP}*)/2+2328, and Write to MEM2 (MEM_CS=2);*
wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]]P0/P0' denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a final write address, MEM_CS is a memory select signal, [[and]]MEM0, MEM1 and MEM2 denote first, second and third memories, respectively, and mod represents a modulo operation.

9. (currently amended) The method of claim 5, wherein if the packet is 3096 or 3864 bits, the write addresses are generated according to at least one formula selected from

i) if 0<TA<N_{EP}*, then*
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0),

ii) if N_{EP}<TA<3xN_{EP}, then

if ((TA-N_{EP}) mod 2=0), then

Input Symbols=P0, WA=(TA-N_{EP})/2, and Write to MEM1 (MEM_CS=1)

else

Input Symbols=P0', WA=(TA-N_{EP})/2, and Write to MEM2 (MEM_CS=2), and

iii) if TA>3xN_{EP}, then

if ((TA-3xN_{EP}) mod 2=1), then

Input Symbols=P1', WA=(TA-3xN_{EP})/2+2328, and Write to MEM1 (MEM_CS=1)

else

Input Symbols=P1, WA=(TA-3xN_{EP})/2+2328, and Write to MEM2 (MEM_CS=2);

wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]] P0/P0'denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a final write address, MEM_CS is a memory select signal, [[and]]MEM0, MEM1 and MEM2 denote first, second and third memories, respectively, and mod represents a modulo operation.

10. (original) The method of claim 1, wherein the demodulation scheme is a multi-level demodulation scheme having a demodulation order of 3 or higher.

11. (previously presented) An apparatus for receiving encoded and then shuffled data in a communication system supporting multi-level demodulation, comprising:

a demodulator for demodulating received data according to a predetermined demodulation scheme and outputting a modulation symbol having a predetermined number of code symbols;

a storage for storing the code symbols in a deshuffling order corresponding to shuffling, the deshuffling order being determined considering the demodulation scheme and the structure of the storage; and

a decoder for reading the stored code symbols, decoding the code symbols at a predetermined code rate, and outputting a packet.

12. (previously presented) The apparatus of claim 11, wherein the storage stores the code symbols at write addresses generated according to a selected one of a plurality of predetermined demodulation schemes using a corresponding one of a plurality of formulas wherein

i) if QPSK, then $WA=(SA+2xmi+ci) \bmod P_{MAX}$,

ii)if 8-PSK, then if $ci=0$, $WA=(SA+mi+2N_{SP}/3) \bmod P_{MAX}$

else $WA=(SA+2xmi+ci-1) \bmod P_{MAX}$, and

iii) if 16-QAM, then if $ci \bmod 2=0$, $WA=(SA+2xmi+ci/2+N_{SP}/2) \bmod P_{MAX}$

else $WA=(SA+2xmi+ci/2) \bmod P_{MAX}$;

wherein WA is a write address, SA is a start address depending on the index of received packet data, mi is the index of a demodulated symbol, ci is the index of a code symbol in the demodulated symbol, N_{SP} is the length of the received packet data, P_{MAX} is the maximum bit index of packet data generated from a code sequence according to an packet size, and mod represents a modulo operation.

13. (original) The apparatus of claim 11, wherein the storage comprises:

a first memory for storing systematic symbols with a relatively high priority among the code symbols;

at least one second memory separate from the first memory, for storing parity symbols with a relatively low priority among the code symbols; and

a write address generator for generating a memory select signal indicating one of the first and second memories each time a code symbol is received and a write address indicating a memory area at which the code symbol is to be stored in the selected memory according to a deshuffling order corresponding to shuffling.

14. (original) The apparatus of claim 13, wherein the write address generator comprises:

a temporary address generator for generating a temporary addresses according to the deshuffling order considering the demodulation scheme; and

a final address generator for generating the memory select signal and the write address using the temporary addresses considering the separate memories.

15. (original) The apparatus of claim 11, wherein the storage comprises:

a first memory for storing systematic symbols with a relatively high priority;

second and third memories separate from the first memory, for storing first and second parity symbols with a relatively low priority;

a temporary address generator for generating a temporary addresses according to the deshuffling order considering the demodulation scheme; and

a final address generator for generating the memory select signal and the write address using the temporary addresses considering the separate memories.

16. (currently amended) The apparatus of claim 15, wherein the temporary address is generated according [[to]]to a selected one of a plurality of predetermined demodulation schemes using a corresponding one of a plurality of formulas wherein

i) if QPSK, then $TA=(SA+2xmi+ci) \bmod P_{MAX}$,

ii)if 8-PSK, then if $ci=0$, $TA=(SA+mi+2N_{SP}/3) \bmod P_{MAX}$

else $TA=(SA+2xmi+ci-1) \bmod P_{MAX}$, and

iii) if 16-QAM, then if $ci \bmod 2=0$, $TA=(SA+2xmi+ci/2+N_{SP}/2) \bmod P_{MAX}$

else $TA=(SA+2xmi+ci/2) \bmod P_{MAX}$;

wherein TA is a temporary address, SA is a start address depending on the index of received packet data, mi is the index of a demodulated symbol, ci is the index of a code symbol in the demodulated symbol, N_{SP} is the length of the received packet data, P_{MAX} is the maximum bit index of packet data generated from a code sequence according to an packet size, and mod represents a modulo operation.

17. (currently amended) The apparatus of claim 15, wherein if the packet is 408, 792 or 1560 bits, the write address is generated by at least one formula selected from

i) if $0<TA<N_{EP}$, *then*
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0),

ii) if $N_{EP}<TA<3xN_{EP}$, *then*
Input Symbols=P0 or P0', WA=TA-N_{EP}, *and Write to MEM1 (MEM_CS=1)*, and

iii) if $3xN_{EP}<TA<5xN_{EP}$, *then*
Input Symbols=P1 or P1', WA=TA-3xN_{EP}, *and Write to MEM2 (MEM_CS=2);*

wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]]P0/P0' denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a final write address, MEM_CS is a memory select signal, [[and]] MEM0, MEM1 and MEM2 denote first, second and third memories, respectively, and mod represents a modulo operation.

18. (currently amended) The apparatus of claim 15, wherein if the packet is 2328 bits, the write address is generated by at least one formula selected from

i) if $0<TA<N_{EP}$, *then*
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0),

ii) if $N_{EP}<TA<3xN_{EP}$, *then*
if ((TA-N_{EP}*) mod 2=0), then*
Input Symbols=P0, WA=(TA-N_{EP}*)/2, and Write to MEM1 (MEM_CS=1)*
else
Input Symbols=P0', WA=(TA-N_{EP}*)/2, and Write to MEM2 (MEM_CS=2)*, and

iii) if $TA>3xN_{EP}$, *then*
if ((TA-3xN_{EP}*) mod 2=1), then*
Input Symbols=P1', WA=(TA-3xN_{EP}*)/2+2328, and Write to MEM1 (MEM_CS=1)*
else

Input Symbols=P1, $WA=(TA-3xN_{EP})/2+2328$, and Write to MEM2 (MEM_CS=2);

wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]]P0/P0' denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a final write address, MEM_CS is a memory select signal, [[and]] MEM0, MEM1 and MEM2 denote first, second and third memories, respectively, and mod represents a modulo operation.

19. (currently amended) The apparatus of claim 15, wherein if the packet is 3096 or 3864 bits, the write address is generated by

i) if $0<TA<N_{EP}$, then
Input Symbols=S, WA=TA, and Write to MEM0 (MEM_CS=0), and

ii) if $TA>N_{EP}$, then
if $((TA-N_{EP}) \bmod 2=0)$,
Input Symbols=P0, $WA=(TA-N_{EP})/2$, and Write to MEM1 (MEM_CS=1)
else
Input Symbols=P0', $WA=(TA-N_{EP})/2$, and: Write to MEM2 (MEM_CS=2);

wherein TA is a temporary address, N_{EP} is an packet size, S denotes systematic symbols, [[P0/P1]]P0/P0' denotes first parity symbols, P1/P1' denotes second parity symbols, WA is a final write address, MEM_CS is a memory select signal, [[and]] MEM0, MEM1 and MEM2 denote first, second and third memories, respectively, and mod represents a modulo operation.

20. (original) The apparatus of claim 11, wherein the demodulation scheme is a multi-level demodulation scheme having a demodulation order of 3 or higher.